REMARKS

Cancellation of Claims 29-32 and 42-60

Applicants have hereby cancelled claims 29-32 and 42-60 to expedite the proceedings in the present application and to place the present application in condition for earlier allowance.

The cancellation of claims 29-32 and 42-60 herein is with express reservation of the right to file a continuation or divisional patent application directed to the subject matter of such cancelled claims, during the pendency of the present application or during the pendency of a further continuation or divisional patent application based on and claiming the priority of the present application.

Response to the Objection to the Information Disclosure Statement

In response to the Examiner's objection to the July 15, 2005 Information Disclosure Statement (IDS) in the October 3, 2005 Office Action, Applicants enclose herewith a new and clearly legible copy of the Kasper reference.

Applicants hereby request that the Examiner consider the Kasper reference, as submitted herewith, which has been recited in the previously submitted July 15, 2005 IDS.

Response to the Objection to Drawings

The Examiner's objection to the drawings of the present application is moot in light of the cancellation of claims 29-32 and 42-60 and the deletion of the limitation "over a layer thickness in the range from about 6 Å to about 60 Å" from the remaining claims 33-41.

Response to §103(a) Rejections of Claims 29-32

The Examiner's rejections of claims 29-32 are moot in light of the cancellation of claims 29-32 herein.

Allowable Claims 33-41

In the October 3, 2005 Office Action, the Examiner stated that claims 33-41 would be allowable if rewritten in independent form and removing the reasons for the objection to the drawings.

Applicants have hereby rewritten the allowable claims 33 and 34, from which claims 35-41 depend, in independent form. Further, Applicants have hereby amended claims 33 and 34 by deleting the limitation "over a layer thickness in the range from about 6 Å to about 60 Å," which renders the objection to the drawings moot.

Therefore, claims 33-41 as amended herein are in condition for allowance.

Issue of a Notice of Allowance for the application is therefore requested. If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,

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Growth of 100 GHz SiGe-Heterobipolar Transistor (HBT) Structures

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The transit frequency f_T of SiGe-heterobipolar transistors (HBT's) was increased from 20 GHz to 100 GHz. This was mainly achieved by thickness reduction of the double heterojunction SiGe-base from 65 nm to 25 nm. The complete vertical structure of the SiGe-HBT's (collector, base, emitter, emitter contact) was grown in one run by Si molecular beam epitaxy (Si-MBE). The growth temperature was varied from 650°C at the collector side to 325°C at the emitter contact side. The different n-type doping levels (10^{17}/cm^3, 10^{18}/cm^3, 10^{20}/cm^3) were obtained by applying three different Sb-doping techniques (secondary implantation, adatom pre build-up, low temperature doping). The p-type base was doped with boron. The doping level in the base (6×10^{19}/cm^3) exceeded the emitter doping level by a factor of 30 (doping level inversion).

KEYWORDS: heterostructure, silicon germanium (SiGe), heterobipolar transistor (HBT), molecular beam epitaxy (MBE), silicon devices, doping, transit frequency, secondary ion mass spectrometry (SIMS), X-ray diffraction (XRD)

1. Introduction

Bipolar junction transistors need an emitter higher doped than the base for the desired emitter efficiency (current gain). The silicon bipolar junction transistor (Si-BJT) is limited in its speed by the base properties (lower limit for the base width w_B, upper limit for the base doping N_B). The principal (punchthrough, tunneling) and technological limits (doping fluctuations, pinch resistivity) are given in Fig. 1 (calculated for flat doping profiles, but similarily valid for general profiles). Punchthrough of the reverse biased collector-base junction occurs for low base sheet dopings. The other limit for the base doping is given by tunneling of the emitter-base junction at roughly $N_B=5\times10^{18}$/cm^3 ($N_E\gg N_B$). The constraints from technological reasons may be even stricter. Consider a thin base with statistically distributed acceptors. Fluctuations and local punchthrough may occur when the number N of acceptors within a cube of length w_B is to small. In Fig. 1 the limit for $N=N_B w_B^3=10$ acceptors is shown. Outside of the active emitter area where the emitter-base junction is not forward biased the space charge layer from this junction may pinch the connection between base contact and inner base. In Fig. 1 the broken line shows the pinch resistivity $R=\infty$ (complete pinching). Finite values of the pinch resistivity are obtained below the broken line. The need for a certain current gain β which can be fulfilled only with high emitter dopings $N_E\gg N_B$ and the above given base layer limitations set the BJT in a unfavorable position. This layer design restriction is eliminated by the concept of the heterobipolar transistor (HBT) where the emitter made from a larger bandgap material provides enough efficiency for a nearly unrestricted choice of the doping levels of emitter and base. A modification of this concept relies on a small band gap base material with a double heterojunction (emitter/base and base/collector). Several groups have now succeeded to realize silicon based heterobipolartransitors with a SiGe base (SiGe-HBT). The layer design freedom gained by the SiGe-HBT can be advantageously used to improve the speed of silicon based transistors. At least three groups demonstrated SiGe-HBT's with $f_T=50$ GHz-91 GHz.[1-3] Very recently[4] an IBM group and our group[5] reported to have overcome the 100 GHz limit.

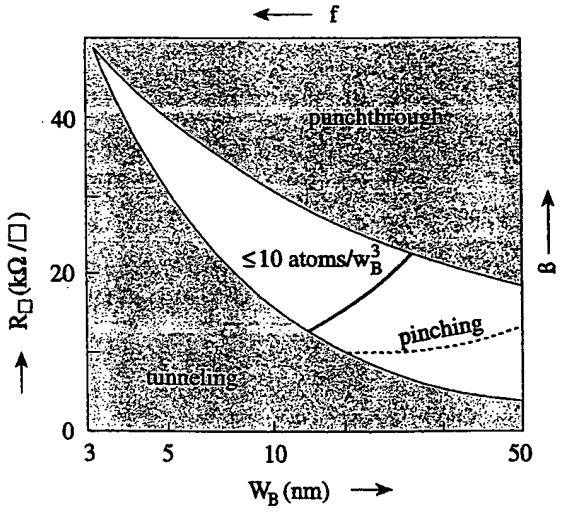

Fig. 1. Base sheet resistivity $R_\square$ versus base width w_B for Si-BJT with flat profiles.

2. Device Fabrication and High Frequency Measurements

The layer designs and the transistor fabrication schemes of the various groups differ considerably with respect to Ge content, Ge grading, base sheet resistivity, growth technique and post epitaxial processing. We try it to classify by the following scheme (Table I). One criterion of the classification is if inversion of the doping levels ($N_B>N_E$) is obtained (true HBT). Especially with strong Ge grading (low Ge content at the B-E junction) the inversion cannot be realized. Other criteria[1-8] involved include selective growth, growth of the complete structure in one run, mesa type device morphology and postepitaxial processing temperatures. A rather large spread is seen in base sheet resistivities (0.7 kΩ/□-17 kΩ/□) with essential improvements compared to BJT only for layer designs

Table I. Technical SiGe-HBT solutions. Provisional classification scheme. See text.

Ref.	Doping inversion	Selective growth	One epi run	Planar (non mesa)	Max. process T
2.	−	−	−	+	conv.
6.	+	−	−	+	880°C, 15 s
4.	?	−	−	+	800°C, 10 s
1.	−	+	−	+	950°C
7.	+	−	+	−	900°C
8.	+	−	+	(−/+)	800°C
3, 5	+	−	+	−	−

with doping level inversion. We used here a processing scheme which is based on:

(i) Growth of the complete structure (collector, base, emitter, emitter contact) in one epitaxy run.

(ii) Simple device definition by double mesa etching.[9]

(iii) No postepitaxial heat processes above 600°C.

This processing scheme allows rather easy and rapid tests of HBT-structures. Typical values of the current gain were 50–250, typical values of the breakdown voltages BV were 4–6 V, 3–5 V, 6–12 V for EB0, CE0, BC0, respectively. Mesa type test transistors (Fig. 2) for on wafer measurements were fabricated without any additional doping or surface passivation steps. Gummel plot measurements in normal and inverse direction were performed and the ideality factors n of the collector currents were very carefully determined. Parasitic barriers at the E-B junction as created by outdiffusion would increase the ideality factor n from 1.0 to up to 1.1. Parasitic barriers at the B-C junction can be seen in inverse operation by an increase of the inverse ideality factor $n_{(i)}$. It can be shown that a simple relationship[10] exists between the Early voltage V_A and the inverse ideality factor

$$V_A = V_T \frac{n_{(i)}}{n_{(i)} - 1} \tag{1}$$

The inverse Early voltage and the normal ideality factor are related in the same way. In our experiments we found out that these electrical measurements are more sensitive to boron outdiffusion (1–2 nm) than secondary ion mass spectrometry (SIMS) analysis (3–5 nm). Furtheron it seems that the (SIMS) boron profile is systematically shifted (~5 nm) to higher depths (knock on effect of the analysing ions?). Guided by these electrical measurements we have chosen the thicknesses of the intrinsic cladding layers to be 1–2 nm (emitter side) and 10–15 nm (collector side), respectively. As a next step we have varied the thicknesses of the SiGe layers from 65 nm to 25 nm. The associated decrease of the base transit time τ_B

$$\tau_B = \frac{w_B^2}{2D} \tag{2}$$

resulted in an increase of the transit frequency f_T (Fig. 3) from 20 GHz to slightly above 100 GHz. Together with an IBM group[4] we demonstrated the first operation of a Si-based transistor at the 100 GHz region. In our case this was obtained—due to the superior base sheet resistivities (0.7 kΩ/□ −3 kΩ/□)—with a simple process and relaxed optical lithography (1 μm emitter contact line). Because of the simple process (no outer base, large collector area) the best f_{max} values obtained with 30 nm SiGe layers are significantly below 100 GHz (best f_{max}=65 GHz). In spite of that this f_{max} value is to our knowledge also a record for SiGe-HBTs.

Encouringing noise measurements[11,12] were reported from these series both for low phase noise (minimum noise figure f_{min}<1.2 dB at 10 GHz) and for low 1/f noise corner frequencies (50 kHz, input noise voltage). Circuit tests were performed with hybrid integrated 24 GHz-oscillators.[13]

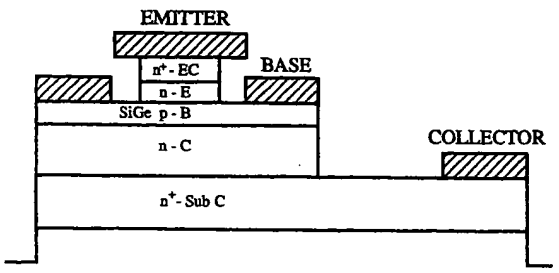

Fig. 2. Scheme of the mesa type HBT.

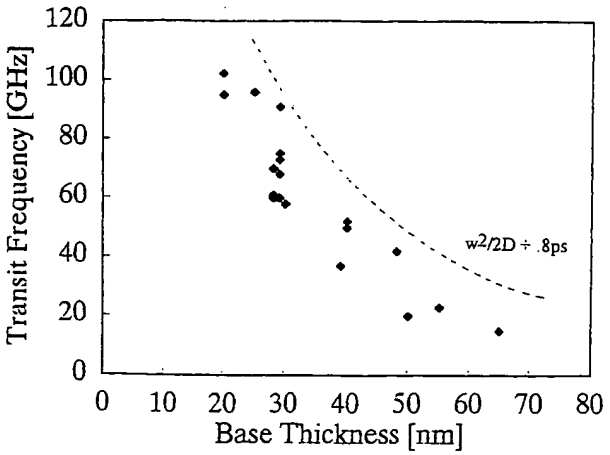

Fig. 3. Measured transit frequency f_T as function of the base thickness w_B. The base thickness is assumed to be equal the SiGe layer thickness.

3. Growth of the Complete Layer Sequence

The complete layer sequence of the SiGe-HBT is grown in one run by MBE on top of a p-substrate with an appropriate n^+-buried layer (arsenic doped with a sheet concentration of $2\times10^{16}/cm^2$). The MBE equipment used (Si-MBE-B) was already decribed.[14] We report about the different doping techniques applied for the realization of the npn transistor and the n^+ emitter contact (the n^+-collector contact is provided by the buried layer). Table II gives an overview about the growth temperatures and the applied doping techniqes

Table II. Growth temperature and doping methods.[15]

Process step	Temperature (°C)	Doping method
Substrate cleaning	900	—
Si collector	650	Sb, DSI
$Si_{1-x}Ge_x$ base	530	B, elemental
Si emitter	450	Sb, PBU
Si emitter contact	325	Sb, LTD
Anneal	600	—

DSI, doping by secondary implantation: LTD, low temperature doping: PBU pre-build-up.

Table III. As-grown layer sequence of the $Si_{1-x}Ge_x$ heterobipolar transistor where the specific values given are from sample B2640.

Function	Thickness	Doping (10^{17}/cm^3)	Ge content x
Collector	130	Sb(4)	0
Cladding	15	i	0, 28
Base	10	B(600)	0, 28
Cladding	2	i	0, 28
Emitter	70	Sb(20)	0
Emitter-contact	230	Sb(2000)	0

which are mainly determined by the selected growth temperature regime. Growth started at 650°C (collector) and finished at 325°C (emitter contact). Before and after growth annealing temperatures of 900°C and 600°C were utilized for substrate cleaning and crystal ordering, respectively. Antimony is used as n-type dopant material.

Si atoms ionized at the electron beam evaporator and accelerated by a substrate voltage of typically few hundred volts helped to incorporate adsorbed Sb atoms at 650°C growth temperature when spontaneous incorporation is nearly negligible. The method is called *doping* by *secondary ions* (DSI). Doping levels of 10^{18}/cm^3 can be obtained by the *pre-build up* (PBU) of a submonolayer Sb adatom layer at lower growth temperatures (450°C) when Sb incorporation is small. Nearly complete incorporation of the impinging Sb atoms is provided at lower growth temperatures (325°C) when segregation of Sb adatoms is suppressed by kinetic reasons (LTD, *low temperature doping*). Boron is used as p-type dopant material. In the equipment used the boron atom beam is generated by evaporation of elemental boron from a special high temperature effusion cell.[12] Boron is easily incorporated at a growth temperature of 530°C.

The general structure of the HBT is shown in Table III. The layer sequence starts with the n-type collector doped with Sb. The highly boron doped base (several 10^{19}/cm^3) is clad on both sides by intrinsic layers with thicknesses of a few nanometer. These intrinsic layers allow for a small segregation or outdiffusion of boron and should therefore be designed in accordance with the complete processing scheme. The following emitter and emitter contact layers are Sb-doped to about 10^{18}/cm^3 and 10^{20}/cm^3, respectively.

In the one series we are mainly reporting here the thicknesses of the SiGe layer were decreased from 65 nm to 25 nm. Simultaneously the thicknesses of the boron doping were decreased from 50 nm to 10 nm. The transit frequencies f_T increased from 20 GHz to 100 GHz partly due to a lower base transit time.

The specific layer parameters of the sample (B2640) with the highest f_T (101 GHz) are summarized in Table III. A very thin intrinsic cladding layer (2 nm) between base and emitter is realized besides the small boron doping layers. SIMS analysis (Fig. 4) essentially confirms a chemical structure which was grown by MBE very similar to the intended one. Furtheron an analytical problem is the measurement of the intrinsic layer widths

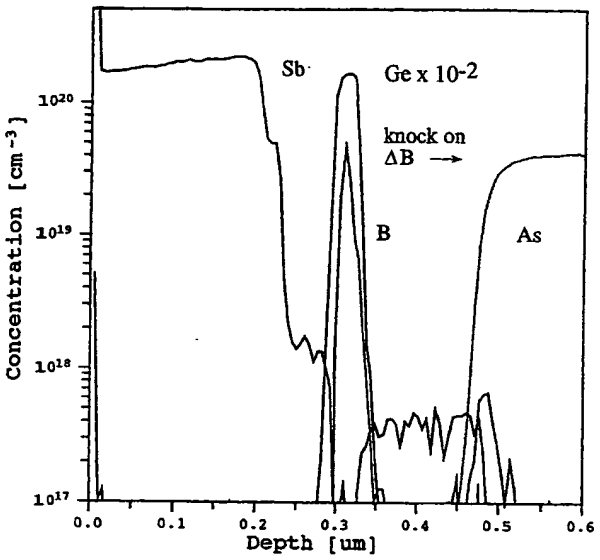

Fig. 4. SIMS profile of sample B2640. From right to left; subcollector (As), collector (Sb), base (Ge·10^{-2}, B), emitter (Sb), emitter contact (Sb).

(cladding layers) and of the boron profile on a nanometer scale.

4. X-Ray Analysis

Bragg-case X-ray diffraction is a powerful fast analytical tool which is extremely employed for characterization of semiconductor heterostructures. The method is highly sensitive to lattice parameter differences, layer thicknesses, and crystal disorder. The Ge lattice constant is 4.2% larger than that of Si. As a first approximation one can assume a linear relationship between Ge content x of the alloy and the lattice mismatch η (Vegard's law):

$$\eta \simeq 0.0042x. \tag{3}$$

For exact calculations the slight deviation[13] from Vegard's law has to be considered

$$\eta = 0.042 \times [1 - 0.12(1-x)]. \tag{4}$$

For the assessment of the HBT's we used a high resolution X-ray diffractometer equipped with a four-crystal monochromator (Philips MPD 1880 HR).

In Fig. 5(a) the rocking curve of the HBT sample B

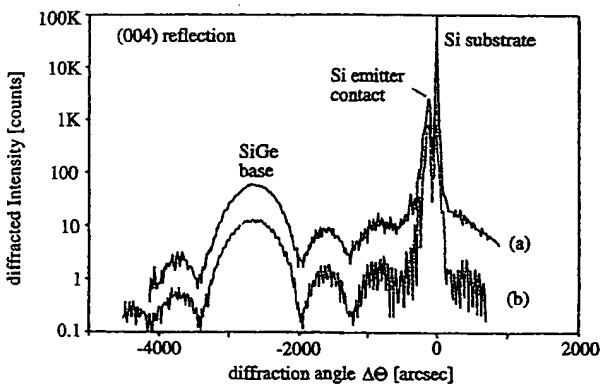

Fig. 5. X-ray diffractions profile from the same structure as in Fig. 1. (a) Measurement, (b) Simulation.

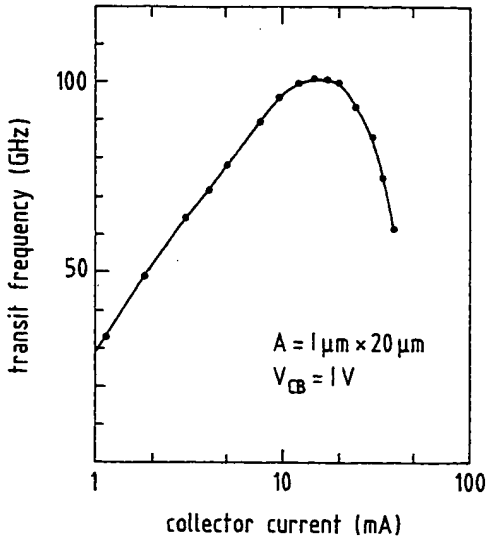

Fig. 6. Transit frequency as function of the collector current. For sample data see Table II.

2640 is given showing well resolved the diffraction lines from the Si substrate, the $Si_{1-x}Ge_x$ base, and the Sb doped, emitter contact layer surrounded by the pendellösung oscillations resulting from the respective layer thicknesses.

Important layer parameters like Ge content in the base and layer thicknesses can be gained by a simple, graphical evaluation of a rocking curve. A full interpretation, however of an experimental diffraction pattern requires the comparison with computer simulations of model structures because with this method additional details like interface sharpness, layer homogeneity and crystal perfection are taken into account. The computer simulation of a model HBT (Fig. 5(b)) consisting of a 27 nm $Si_{0.715}Ge_{0.285}$ base, a 75 nm Si emitter, and a 235 nm thick Si contact cap ($\sim 3\times10^{20}/cm^3$ Sb doped) yields a virtually perfect fit to the experimental curve indicating excellent structural quality.

5. Conclusion

We have grown the complete HBT layer and doping structure (collector, base, emitter, emitter contact) in one run by a Si-MBE process. The substrate temperature was chosen to decrease from 650°C to 325°C during growth. The excellent electronic quality of this structure was proven by the fabrication of high frequency SiGe-HBTs with f_T ranging from 20 GHz to 100 GHz (Fig. 6). The increase in f_T beyond the silicon transistor limits was obtained by a systematic decrease of the SiGe layer thickness from 65 nm to 25 nm. Simultaneously a high boron doping level ($6\times10^{19}/cm^3$) of the base yielded extremely low base sheet resistivities (0.7 kΩ/□ for f_T=50 GHz, 2.6 kΩ/□ for f_T=100 GHz). Good prospects for further rapid progress are expected because the given approach is based on flat profiles within each layer.

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